

WHAT IS CLAIMED IS:

1 1. A solid state image sensor comprising:
2 a semiconductor substrate having an imaging area and a
3 peripheral area defined thereon so that said peripheral area
4 surrounds said imaging area;
5 a field isolation dielectric formed as isolation regions
6 on said substrate in said peripheral area;
7 a gate insulating film formed on said substrate in said
8 imaging area and surrounded by said field isolation dielectric;
9 a plurality of vertical and horizontal shift register
10 electrodes formed on said gate insulating film in said imaging
11 area and on said field isolation dielectric in said peripheral
12 area, said plurality of vertical and horizontal shift register
13 electrodes being made from a single layer of conductor;
14 photoelectric conversion elements formed in said
15 substrate, each element being surrounded by said vertical shift
16 register electrode;
17 an interlayer insulation film having a planarized surface
18 and covering said plurality of vertical and horizontal shift
19 register electrodes, as well as gaps between said plurality of
20 vertical and horizontal shift register electrodes, said
21 interlayer insulation film being formed on said gate insulating
22 film on each of said photoelectric conversion elements and formed
23 lower than said vertical shift register electrode on each of
24 said photoelectric conversion elements; and
25 a light shielding metal layer provided on said interlayer
26 insulation film on said plurality of vertical and horizontal
27 shift register electrodes and having openings above said
28 photoelectric conversion elements, said light shielding metal
29 layer serving as interconnects for making electrical connection

30 to said plurality of vertical and horizontal shift register
31 electrodes in said peripheral area.

1 2. The solid state image sensor according to claim 1,
2 wherein a distance between adjacent electrodes out of said
3 plurality of vertical and horizontal shift register electrodes
4 in said peripheral area is larger than a distance between adjacent
5 electrodes out of said plurality of first and second shift
6 register electrodes in said imaging area.

1 3. The solid state image sensor according to claim 1,
2 wherein said interlayer insulation film on said plurality of
3 vertical and horizontal shift register electrodes in said imaging
4 area is thinner than said interlayer insulation film on said
5 plurality of vertical and horizontal shift register electrodes
6 in said peripheral area.

1 4. The solid state image sensor according to claim 1,
2 wherein said interlayer insulation film on said plurality of
3 vertical and horizontal shift register electrodes in said
4 peripheral area and said interlayer insulation film on said
5 plurality of second shift register electrodes in said imaging
6 area have the same thickness and wherein said interlayer
7 insulation film on said plurality of first shift register
8 electrodes in said imaging area is thinner than said interlayer
9 insulation film on said plurality of vertical and horizontal
10 shift register electrodes in said peripheral area.

1 5. The solid state image sensor according to claim 1,
2 wherein said plurality of vertical shift register electrodes
3 in said imaging area serve as a readout electrode used to transfer

4 electrical charge generated in each of said photoelectric
5 conversion elements to a shift register channel below said
6 plurality of vertical shift register electrodes.

1 6. The solid state image sensor according to claim 1,
2 further comprising a vertical shift register channel below said
3 plurality of vertical shift register electrodes and a horizontal
4 shift register channel below said plurality of horizontal shift
5 register electrodes.

1 7. The solid state image sensor according to claim 1,
2 wherein a surface portion of said plurality of vertical and
3 horizontal shift register electrodes in said imaging area is
4 a silicide layer.

1 8. A solid state image sensor comprising:
2 a semiconductor substrate having an imaging area and a
3 peripheral area defined thereon so that said peripheral area
4 surrounds said imaging area;
5 a field isolation dielectric formed as isolation regions
6 on said substrate in said peripheral area;
7 a gate insulating film formed on said substrate in said
8 imaging area and surrounded by said field isolation dielectric;
9 a plurality of shift register electrodes formed on said
10 gate insulating film in said imaging area and on said field
11 isolation dielectric in said peripheral area;
12 photoelectric conversion elements formed in said
13 substrate in said imaging area, each element being surrounded
14 by said shift register electrode; and
15 an interlayer insulation film having a planarized surface
16 and covering said plurality of shift register electrodes, as

17 well as gaps between said plurality of shift register electrodes,
18 said interlayer insulation film being formed on said gate
19 insulating film on each of said photoelectric conversion elements
20 and formed lower than said shift register electrode surrounding
21 each of said photoelectric conversion elements.

1 9. The solid state image sensor according to claim 8,
2 wherein said plurality of shift register electrodes are made
3 from a single layer of conductor.

1 10. The solid state image sensor according to claim 8,
2 wherein a distance between adjacent electrodes out of said
3 plurality of shift register electrodes in said peripheral area
4 is larger than a distance between adjacent electrodes out of
5 said plurality of shift register electrodes in said imaging area.

1 11. The solid state image sensor according to claim 8,
2 further comprising a light shielding metal layer provided on
3 said interlayer insulation film on said plurality of shift
4 register electrodes, wherein said light shielding metal layer
5 has openings above said photoelectric conversion elements and
6 serves as interconnects for making electrical connection to said
7 plurality of shift register electrodes in said peripheral area.

1 12. The solid state image sensor according to claim 8,
2 wherein said plurality of shift register electrodes comprises
3 a plurality of vertical and horizontal shift register electrodes
4 and wherein said plurality of vertical shift register electrodes
5 are disposed adjacent said photoelectric conversion elements
6 to retrieve electrical charge generated in said photoelectric
7 conversion elements.

1 13. The solid state image sensor according to claim 12,
2 wherein said interlayer insulation film covers said plurality
3 of vertical and horizontal shift register electrodes and gaps
4 between said plurality of vertical and horizontal shift register
5 electrodes and wherein said interlayer insulation film on said
6 plurality of vertical and horizontal shift register electrodes
7 in said imaging area is thinner than said interlayer insulation
8 film on said plurality of vertical and horizontal shift register
9 electrodes in said peripheral area.

1 14. The solid state image sensor according to claim 12,
2 wherein said interlayer insulation film covers said plurality
3 of vertical and horizontal shift register electrodes, as well
4 as gaps between said plurality of vertical and horizontal shift
5 register electrodes in said imaging area and wherein said
6 interlayer insulation film on said plurality of vertical and
7 horizontal shift register electrodes in said peripheral area
8 and said interlayer insulation film on said plurality of
9 horizontal shift register electrodes are the same in thickness,
10 and wherein said interlayer insulation film on said plurality
11 of vertical shift register electrodes in said imaging area is
12 thinner than said interlayer insulation film on said plurality
13 of vertical and horizontal shift register electrodes in said
14 peripheral area.

1 15. The solid state image sensor according to claim 12,
2 further comprising a vertical shift register channel below said
3 plurality of vertical shift register electrodes and a horizontal
4 shift register channel below said plurality of horizontal shift
5 register electrodes.

1 16. The solid state image sensor according to claim 12,
2 wherein a surface portion of said plurality of vertical and
3 horizontal shift register electrodes is silicide layer.

1 17. A solid state image sensor comprising:
2 a semiconductor substrate having an imaging area and a
3 peripheral area surrounding said imaging area;
4 a field isolation dielectric formed on said peripheral
5 area to define said imaging area;
6 a plurality of photoelectric conversion elements formed
7 in said imaging area, each of said photoelectric conversion
8 elements having an insulating film formed on an associated part
9 of said imaging area;
10 a charge transfer section provided in said imaging area
11 to transfer charges generated by said photoelectric conversion
12 elements, said charge transfer section having a plurality of
13 shift register electrodes, each of shift register electrodes
14 being elongated over said field isolation dielectric to form
15 an elongated portion;
16 an interlayer insulation film covering the elongated
17 portion of said each of said shift register electrodes so that
18 said interlayer insulation film in said peripheral area is
19 thicker than said insulating film of each of said photoelectric
20 conversion elements; and
21 a conductive layer formed on said interlayer insulation
22 film to cross the elongated portion of said each of said shift
23 register electrodes.

1 18. The solid state image sensor according to claim 17,
2 wherein said plurality of shift register electrodes are made

3 from a single layer of conductor.

1 19. The solid state image sensor according to claim 17,
2 wherein the elongated portions of said shift register electrodes
3 are arranged such that a distance between adjacent elongated
4 portions in said peripheral area is larger than a distance between
5 adjacent elongated portions in said imaging area.

1 20. The solid state image sensor according to claim 17,
2 wherein said charge transfer section comprises vertical and
3 horizontal charge transfer sections and wherein said interlayer
4 insulation film on said elongated portions in said horizontal
5 charge transfer section and said interlayer insulation film on
6 said elongated portions in said peripheral area are the same
7 in thickness, and wherein said interlayer insulation film on
8 said elongated portions in said vertical charge transfer section
9 is thinner than said interlayer insulation film on said elongated
10 portions in said peripheral area.